CLAIMS

1. A phase change memory device, comprising:

a memory array formed by a plurality of memory cells, each memory cell comprising a memory element of calcogenic material and a selection element connected in series to said memory element;

a plurality of address lines connected to said memory cells; and

a write stage connected to said memory array, said write stage including current generator means selectively connected to said address lines and supplying selected memory cells with preset currents having values that modify an electrical property of the memory element of said selected memory cells.

2. The memory device according to claim 1 wherein said write stage comprises a single current generator that is connected to said address lines.

3. The memory device according to claim 1 wherein said write stage comprises a plurality of current generator circuits, one for each selected address line connected to an addressed memory cell.

4. The memory device according to claim 3 wherein each current generator circuit comprises:

a plurality of generator transistors each having a control terminal receiving a respective control signal and an output terminal;

a load circuit having an input connected to said output terminals of said generator transistors and an output connected to a respective selected address line; and

a logic circuit having a data input receiving a data signal and a plurality of outputs connected respectively to the control terminals of said generator transistors and generating said control signals according to said data signal.

5. The memory device according to claim 3 wherein each current generator circuit comprises:

a generator transistor having a control terminal receiving a control signal and an output terminal;

a load circuit having an input connected to said output terminal of said generator transistor and an output connected to a respective selected address line; and

a logic circuit having a data input receiving a data signal and an output connected to said control terminal of said generator transistor and generating said control signal of value correlated to said data signal.

6. The memory device according to claim 1, further comprising a read stage connected to said memory array, said read stage comprising:

voltage generator means connected to selected address lines for biasing said selected address lines at a preset read voltage and causing cell currents to flow in selected memory cells; and

comparator means connected to said selected address lines and comparing said cell currents with reference currents of preset value.

7. The memory device according to claim 6, further comprising an operation selector stage connected to said read stage, write stage and memory array for selectively connecting said selected address lines to said write stage and comparator means of said reading stage.

8. The memory device according to claim 6 wherein said comparator means comprise a dual-input dynamics differential circuit.

9. The memory device according to claim 6 wherein said comparator means comprise, for each selected address line:

a first subtractor element connected to a respective one of said selected address lines and to a reference line and generating an output voltage proportional to the difference between a cell current flowing in said respective selected address line and a reference current flowing in said reference line;

a second subtractor element connected to said respective selected address line and to said reference line and generating an output voltage proportional to the difference between said reference current and said flowing cell current, and

a differential amplifier connected to said first and to said second subtractor elements.

10. The memory device according to claim 9 wherein said comparator means further comprise:

a cell mirror circuit having an input connected to said respective address line; a first and a second output supplying a current correlated to said cell current, said first output of said cell mirror circuit being connected to said first subtractor element;

a reference current mirror circuit having an input connected to said reference line; a first and a second output supplying a current correlated to said reference current, said first output of said reference mirror circuit being connected to said second subtractor element;

a first mirror circuit connected between said second output of said cell mirror circuit and said second subtractor element; and

a second mirror circuit connected between said second output of said reference mirror circuit and said first subtractor element.

11. A method for writing a phase change memory device that includes a memory array, formed by of a plurality of memory cells each including a memory

element of calcogenic material and a selection element connected in series, the method comprising:

determining that a selected one of said memory cells is desired to be written to; and

supplying the selected one of said memory cells with a preset current having a value modifying an electrical property of the memory element of said selected memory cell.

12. The writing method according to claim 11 wherein said supplying step comprises supplying the selected one of said memory cells with a plurality of current pulses.

13. The writing method according to claim 12 wherein said pulses have an increasing amplitude when modifying said electrical property in a first direction and a decreasing amplitude when modifying said electrical property in a second direction, opposite to said first direction.

14. The writing method according to claim 12 wherein after applying each pulse, the method includes:

reading the selected one of the memory cells for verifying said electrical property;

generating a cell signal proportional to a value of said electrical property;

comparing said cell signal with a desired value; and

applying a subsequent current pulse only if said cell signal has a preset relation with said desired value.

15. The writing method according to claim 11, further comprising reading the selected memory cell by the steps of biasing an address line connected to said selected memory cell at a preset read voltage, detecting a cell current flowing in

said selected memory cell, and comparing said cell current with a reference current of preset value.

16. The writing method according to claim 15 wherein said step of comparing comprises generating a first voltage signal proportional to the difference between said cell current and said reference current; generating a second voltage signal proportional to the difference between said reference current and said cell current; and comparing said first and second signals through a differential amplifier.

17. A phase change memory device, comprising:

a memory array formed by rows and columns of memory cells, each memory cell comprising a memory element of calcogenic material and a selection element connected in series to the memory element;

a plurality of bit lines connected respectively to the columns of memory cells; and

a write stage connected to the memory array, the write stage including current generator selectively connected to a selected one of the bit lines and supplying a selected one of the memory cells connected to the selected bit line with a preset current having a value that modifies an electrical property of the selected memory cell, the current generator being structured to ensure that the value of the preset current does not depend on a position of the selected memory cell within the column to which the selected bit line is connected.

18. The memory device according to claim 17 wherein the current generator is connected to a plurality of the bit lines.

19. The memory device according to claim 17 wherein the write stage comprises a plurality of current generator circuits, one for each of the bit lines.

20. The memory device according to claim 17 wherein the current generator comprises:

a plurality of generator transistors each having a control terminal receiving a respective control signal and an output terminal;

a load circuit having an input connected to the output terminals of the generator transistors and an output connected to the selected bit line; and

a logic circuit having a data input receiving a data signal and a plurality of outputs connected respectively to the control terminals of the generator transistors and generating the control signals according to the data signal.

21. The memory device according to claim 17 wherein the current generator comprises:

a generator transistor having a control terminal receiving a control signal and an output terminal;

a load circuit having an input connected to the output terminal of the generator transistor and an output connected to a the selected bit line; and

a logic circuit having a data input receiving a data signal and an output connected to the control terminal of the generator transistor and generating the control signal of value correlated to the data signal.

22. The memory device according to claim 17, further comprising a read stage connected to the memory array, the read stage comprising:

a voltage generator connected to the selected bit line for biasing the selected bit line at a preset read voltage and causing a cell current to flow in the selected memory cell; and

a comparator connected to the selected bit line and structured to compare the cell current with a reference current of preset value.

23. The memory device according to claim 22 wherein the comparator comprises a dual-input dynamics differential circuit.

24. The memory device according to claim 22 wherein the comparator comprises:

a first subtractor element connected to the selected bit line and to a reference line and generating an output voltage proportional to the difference between a cell current flowing in the selected bit line and a reference current flowing in the reference line;

a second subtractor element connected to the selected bit line and to the reference line and generating an output voltage proportional to the difference between the reference current and the flowing cell current, and

a differential amplifier connected to the first and to the second subtractor elements.

25. The memory device according to claim 24 wherein the comparator further comprises:

a cell mirror circuit having an input connected to the select bit line; a first and a second output supplying a current correlated to the cell current, the first output of the cell mirror circuit being connected to the first subtractor element;

a reference current mirror circuit having an input connected to the reference line; a first and a second output supplying a current correlated to the reference current, the first output of the reference mirror circuit being connected to the second subtractor element;

a first mirror circuit connected between the second output of the cell mirror circuit and the second subtractor element; and

a second mirror circuit connected between the second output of the reference mirror circuit and the first subtractor element.